This listing of claims replaces all prior versions and listings of the claims in the application.

In the Claims

1. (currently amended) A conductor line stack, comprising:

a first layer consisting essentially of at least one ~~a~~ first material selected from the group consisting of polysilicon and metal silicides;

a second layer consisting essentially of ~~a~~ at least one second material formed on said first layer ~~of first material~~, said second layer ~~of second material~~ having an upper portion and a lower portion; and

a pair of first spacers disposed on sidewalls of said upper portion, said lower portion having width defined by a combined width of said upper portion and said pair of first spacers.

2. (canceled)

3. (currently amended) The conductor line stack of claim ~~2~~ 1, wherein said second material includes a metal.

4. (currently amended) The conductor line stack of claim 1, ~~wherein said conductor line stack~~ further ~~comprises~~ comprising an insulating cap disposed over said second layer ~~of second material~~, and second spacers disposed on sidewalls of said first spacers, on sidewalls of said lower portion and on sidewalls of said first layer ~~of said first material~~.

5. (original) A conductor contact structure including a conductor line stack as claimed in claim 4, further comprising a borderless bitline contact to a single-crystal semiconductor region disposed below said conductor line stack, said bitline contact having a sidewall contacting a sidewall of said second spacer.

6. (currently amended) A conductor contact structure including a pair of conductor line stacks as claimed in claim 4, said conductor line stacks being oriented in parallel, said conductor contact structure ~~further comprising~~including a borderless bitline contact to a single-crystal semiconductor region disposed below said pair of conductor line stacks, said bitline contact contacting sidewalls of said second spacers of said conductor line stacks.

7. (original) The conductor contact structure of claim 6 wherein said borderless bitline contact includes heavily doped polysilicon.

8. (canceled)

9. (currently amended) The conductor contact structure of claim ~~8~~ 6 wherein a first ~~a~~ conductor line stack of said pair of conductor line stacks is separated from said single-crystal semiconductor region by an array top oxide layer and ~~another~~ a second conductor line stack of said pair of conductor line stacks is conductively coupled to a gate conductor of a vertical passgate transistor of a dynamic random access memory.

10. (currently amended) A conductor contact structure comprising:

a pair of conductor line stacks oriented in parallel, each said conductor line stack including:

a first layer consisting essentially of ~~a~~ at least one first material selected from the group consisting essentially of ~~heavily~~ doped polysilicon ~~and a metal silicide~~;

a second layer consisting essentially of at least one material selected from the group consisting of metals and metal silicides ~~metal formed over~~ overlying said first layer ~~of first material~~, said second layer ~~of metal~~ having an upper portion and a lower portion;

an insulating cap formed over said second layer ~~of metal~~; and

a pair of first spacers disposed on sidewalls of said upper portion and said insulating cap, said lower portion having width defined by a combined width of said upper portion and said pair of first spacers; and

a pair of second spacers disposed on sidewalls of said first spacers, on sidewalls of said lower portion and on sidewalls of said first layer ~~of first material~~;

a borderless bitline contact to a single-crystal semiconductor region disposed below said pair of conductor line stacks, said bitline contact contacting sidewalls of said second spacers of said conductor line stacks,

wherein a first conductor line stack of said pair of conductor line stacks is separated from said single-crystal semiconductor region by an array top oxide layer and

~~another~~ a second conductor line stack of said pair of conductor line stacks is conductively coupled to a gate conductor of a vertical passgate transistor of a dynamic random access memory.

11-20. (canceled)

21. (new) A conductor line stack, comprising:

a first layer consisting essentially of a doped polysilicon;

a second layer disposed on said first layer, said second layer consisting essentially of at least one second material selected from the group consisting of metals and conductive compounds of metals, said second layer having an upper portion and a lower portion; and

a pair of first spacers disposed on sidewalls of said upper portion, said lower portion having width defined by a width of said upper portion combined with a width of said pair of first spacers.

22. (new) The conductor line stack of claim 21, further comprising an insulating cap disposed over said second layer, and second spacers disposed on sidewalls of said first spacers, on sidewalls of said lower portion and on sidewalls of said first layer.

23. (new) A conductor contact structure including a conductor line stack as claimed in claim 22, further comprising a borderless bitline contact to a single-crystal

semiconductor region disposed below said conductor line stack, said bitline contact having a sidewall contacting a sidewall of said second spacer.

24. (new) A conductor contact structure including a pair of conductor line stacks as claimed in claim 22, said conductor line stacks being oriented in parallel, said conductor contact structure including a borderless bitline contact to a single-crystal semiconductor region disposed below said pair of conductor line stacks, said bitline contact contacting sidewalls of said second spacers of said conductor line stacks.

25. (new) The conductor contact structure of claim 24, wherein said borderless bitline contact includes doped polysilicon.

26. (new) The conductor contact structure of claim 24, wherein a first conductor line stack of said pair of conductor line stacks is separated from said single-crystal semiconductor region by an array top oxide layer and a second conductor line stack of said pair of conductor line stacks is conductively coupled to a gate conductor of a vertical passgate transistor of a dynamic random access memory.